Please add the following claim:

65. (New) The method of claim 1, wherein depositing a seed layer includes forming a discontinuous seed layer having island structures with the island structures having a thickness in a range of 3 to 10 nanometers.

REMARKS

Claims 13, 19, 20, 21, 24, 28, 34, and 40 are amended, no claims are canceled, and claim 65 is added; as a result, claims 1-42 and 65 are now pending in this application.

Claim Objections

Claims 13-42 were objected to because of informalities. Specifically, the Office Action objected to the use of the same term "number" to describe different features. Claims 13, 19, 20, 21, 24, 28, 34, and 40 are amended to clarify the term "number" as it relates to different features. These amendments are not made for purposes of patentability under a section of title 35 of the United States Code. Withdrawal of the objection is requested.

§103 Rejection of the Claims

Claims 1-12 were rejected under 35 U.S.C. § 102(e) as being unpatentable over Tan et al. (U.S. Patent No. 6,372,622) in view of Bernier et al. ("Laser Processing of Palladium..."). Applicant respectfully traverses.

Applicant does not admit that the Tan patent is prior art to the present invention and reserves the right to swear behind this patent at a later date. Nevertheless, Applicant also submits that the present invention is distinguishable over the Tan patent in view of Bernier.

The Office Action indicates that the statutory basis for the above rejection is 35 U.S.C. § 102(e). Applicant believes that this is merely a clerical error and responds as if the rejection was made under 35 U.S.C. § 103. If this is not correct, applicant requests that a new Office Action be issued.

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The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d (BNA) 1596, 1598 (Fed. Cir. 1988). In combining prior art references to construct a *prima facie* case, the Examiner must show some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art that would lead an individual to combine the relevant teaching of the references. *Id.* The M.P.E.P. contains explicit direction to the Examiner that agrees with the *In re Fine* court:

> To establish a prima facie case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d (BNA) 1438 (Fed. Cir. 1991)).

An invention can be obvious even though the suggestion to combine prior art teachings is not found in a specific reference. *In re Oetiker*, 977 F.2d 1443, 24 U.S.P.Q.2d (BNA) 1443 (Fed. Cir. 1992). However, while it is not necessary that the cited references or prior art specifically suggest making the combination, there must be some teaching somewhere which provides the suggestion or motivation to combine prior art teachings and applies that combination to solve the same or similar problem which the claimed invention addresses. One of ordinary skill in the art will be presumed to know of any such teaching. (See, e.g., *In re Nilssen*, 851 F.2d 1401, 1403, 7 U.S.P.Q.2d 1500, 1502 (Fed. Cir. 1988) and *In re Wood*, 599 F.2d 1032, 1037, 202 U.S.P.Q. 171, 174 (C.C.P.A. 1979)). However, the level of skill is not that of the person who is an innovator but rather that of the person who follows the conventional wisdom in the art. *Standard Oil Co. v. American Cyanamid Co.*, 774 F.2d 448, 474, 227 U.S.P.Q. 293, 298 (Fed. Cir. 1985). The requirement of a suggestion or motivation to combine references in a *prima facie* case of obviousness is emphasized in the Federal Circuit opinion, *In re Sang Su Lee*, 277 F.3d 1338; 61 U.S.P.Q.2D 1430 (Fed. Cir. 2002), which indicates that the motivation must be supported by evidence in the record.

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The test for obviousness under § 103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved by the combination of elements that define the invention. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 U.S.P.Q. 543, 551 (Fed. Cir. 1985). The Examiner can only rely on references which are either in the same field as that of the invention, or if not in the same field, the references must be "reasonably pertinent to the particular problem with which the inventor was concerned." *M.P.E.P.* § 2141.01 (a) (citing *In re Oetiker*, 24 U.S.P.Q.2d (BNA) 1443 at 1445). The Examiner must also recognize and consider not only the similarities but also the critical differences between the claimed invention and the prior art. *In re Bond*, 910 F.2d 831, 834, 15 U.S.P.Q.2d (BNA) 1566, 1568 (Fed. Cir. 1990), *reh'g denied*, 1990 U.S. App. LEXIS 19971 (Fed. Cir. 1990).

If the proposed modification renders the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *M.P.E.P.* § 2143.01 (citing *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984)). The Examiner must also avoid hindsight. *Id.* The Examiner cannot use the Appellant's structure as a "template" and simply select elements from the references to reconstruct the claimed invention. *In re Gorman,* 933 F.2d 982, 987, 18 U.S.P.Q.2d (BNA) 1885, 1888 (Fed. Cir. 1991).

Applicant submits that a *prima facie* case of obviousness has not been established. The Office Action states that a person of ordinary skill is motivated to modify Tan with Bernier to use electroless plating to deposit Cu to obtain a simpler and less costly process. Applicant can not find where Tan or Bernier suggest to one of skill in the art that such a modification would result in a simpler and less costly process. There must be some teaching somewhere which provides the suggestion or motivation to combine prior art teachings and applies that combination to solve the same or similar problem which the claimed invention addresses. Accordingly, the there is no motivation to modify Tan with Bernier.

Applicant respectfully submits that the Examiner may be relying on hindsight. It is well settled that the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention. The present application states

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> The present invention provides for a multilayer copper wiring structure by electroless, selectively deposited copper in a streamlined process which will not require chemical mechanical planarization (CMP). Thus, the present invention significantly reduces the amount of deposited conductive material, e.g. copper, which is ultimately discarded according to conventional processes. This alleviates important environmental concerns regarding the disposition of used materials. Further, by avoiding the need for a CMP process step, the usage of consumables such as pads and slurry is conserved.[1]

Thus, the present invention uses a simpler and less costly process. Applicant believes that the examiner is using the Appellant's disclosure as a "template" and simply select elements from the references to reconstruct the claimed invention. This is not permitted.

One of skill in the art would not be motivated to modify Tan with Bernier as Tan explicitly teaches away from the presently claimed invention. More specifically, Tan states that its seed layer is for electroplating.[2] Thus, Tan teaches away from the present invention as recited in independent claims 1, 7, 8, 13, 20, 28, and 34, which each recite electroless plating.

Applicant further submits that one of skill in the art would not look to Bernier for a teaching of electroless plating that can be combined with Tan. Bernier teaches a complex laser processing of a resin that contains palladium to form a seed layer. Bernier admits that its laser technique used on polyimide results in substrate deterioration (page 331 and 333). Bernier further admits that its laser technique has poor palladium adhesion to a Si_3N_4 substrate (page 333). Thus, one of skill in the art would not look to the teachings of Bernier to modify Tan as Bernier's techniques have admitted faults.

Based at least on the above, applicant respectfully submits that a *prima facie* case of obviousness has not been made. Reconsideration of all claims is respectfully requested.

Turning now to claim 2, applicant respectfully traverses. The Office Action states that any variation in thickness in the present claims is obvious in light f the cited art, because the changes in thickness produce no unexpected function. However, if one does not know which variables are result-effective, then the process cannot be optimized. The C.C.P.A. recognized

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[1] Specification Page 4, lines 19-26

[2] Tan, U.S. Pat. No. 6,372,622, col. 3, line 46.

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this exception when it stated that "If it could be held that the skilled chemist would never think to reduce the temperature or increase the acid concentration, then it might be held that invention resides in so doing." See In re Aller, 220 F.2d 454 (C.C.P.A. 1955). In the instant case, applicant can not find where Tan discusses thickness of a seed layer on barrier layer 14. If a subject is never discussed, it is impossible to "optimize" a related variable. Reconsideration and withdrawal of the rejection of claim 2 are respectfully requested.

Turning now to claim 3, applicant respectfully traverses. Tan and Bernier, either alone of in combination, do not teach depositing a seed layer using a physical vapor deposition process and depositing a layer of copper over the seed layer using electroless plating. Reconsideration and withdrawal of the rejection of claim 2 are respectfully requested.

Turning now to claim 5, applicant respectfully traverses. The Office Action cites Figure 3 of Tan for a showing of filling the number of via holes to a top surface of the photoresist layer. However, Tan's Figure 3 clearly shows the copper layer 30 being beneath the top surface of photoresist layer 31. Bernier does not teach the use of photoresists. Accordingly, claim 5 is allowable over Tan and Bernier, either alone or in combination. Reconsideration and withdrawal of the rejection of claim 5 are respectfully requested.

Turning now to claim 6, applicant respectfully traverses. The Examiner takes Official Notice that plasma ashing is a conventional method of removing photoresist. Applicant respectfully traverses this official notice and requests the Examiner to provide a reference that describes such an element. Absent a reference, it appears that the Examiner is using personal knowledge, so the Examiner is respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

Turning now to claim 8, applicant respectfully traverses. The Examiner takes Official Notice that it is well known in the art that for electroless plating a discontinuous seed layer is used. Applicant respectfully traverses this official notice and requests the Examiner to provide a reference that describes such an element. Absent a reference, it appears that the Examiner is using personal knowledge, so the Examiner is respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

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Applicant submits that all of claims 1-12 are allowable over Tan and Bernier for the various reasons stated above. Allowance of claims 1-12 is requested.

§103 Rejection of the Claims

Claims 13-27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tan et al. in view of Bernier et al. and Simpson (U.S. Patent No. 6,197,688). Applicant respectfully traverses.

Applicant does not admit that the Simpson patent is prior art to the present invention and reserves the right to swear behind this patent at a later date. Nevertheless, Applicant also submits that the present invention is distinguishable over Tan in view of Bernier and Simpson.

Claims 13-27 are believed to be allowable over Tan and Bernier for substantially similar reasons as stated above. Simpson does not cure the defects of Tan and Bernier as references against claims 13-27. Simpson discloses using electroplating to deposit copper layer 34, which is then patterned into copper interconnects 38. In contrast to Tan, Bernier, and Simpson, claim 13 recites forming a first layer of copper using electroless plating, ..., and forming a second layer of copper using electroless plating. Tan, Bernier and Simpson do not teach using electroless plating to form two different layers. Applicant submits that Tan, Bernier and Simpson do not teach all of the features of claim 13. According, applicant requests reconsideration and allowance of claim 13 and claims 14-19 depending from claim 13.

Turning now to claim 14, applicant respectfully traverses. Tan, Bernier and Simpson, either alone or in combination, do not teach depositing a first seed layer that has a discontinuous island structure. It appears that the Examiner is taking Official Notice of this feature. Applicant respectfully traverses this official notice and requests the Examiner to provide a reference that describes such an element. Absent a reference, it appears that the Examiner is using personal knowledge, so the Examiner is respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

Turning now to claim 15, applicant respectfully traverses. The Examiner takes Official Notice that the first layer is deposited by evaporation. Applicant respectfully traverses this official notice and requests the Examiner to provide a reference that describes such an element.

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Absent a reference, it appears that the Examiner is using personal knowledge, so the Examiner is respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

With respect to remaining claims 16-27 and 34-37, applicant submits that they are allowable for substantially the same reasons as stated above. With respect to any official notice, applicant traverses and requests a reference that teaches such a feature.

Claims 28-33 and 38-42 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tan et al. in view of Bernier et al. , Simpson, and Tomita et al. (U.S. Patent No. 5,034,799). Applicant respectfully traverses for at least the reasons stated above. Tomita does not sure the deficiencies of Tan, Bernier and Simpson as references against claims 28-33 and 38-42. Applicant submits that claims 28-33 and 38-42 are allowable for substantially similar reasons as stated above.

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CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

KIE Y. AHN ET AL.

By their Representatives,

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Date 16 Sept. 2002 By _____
Timothy B. Clise
Reg. No. 40,987

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 16th (Mon) day of September, 2002.

Tina Kdraut
Name

_____
Signature

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Docket No. 303.672US1 Micron Ref. No. 99-0715
WD # 453362

CLEAN VERSION OF PENDING CLAIMS

SELECTIVE ELECTROLESS-PLATED COPPER METALLIZATION
Applicant: Kie Y. Ahn et al.
Serial No.: 09/483,881

Claims 1-42 and 65, as of September 16, 2002 (Date of Response to First Office Action).

1. A method for forming copper vias on a substrate, comprising:

depositing a seed layer including a thin film of Palladium (Pd) or Copper (Cu) on the substrate;

using a photolithography technique in order to define a number of via holes above the seed layer; and

depositing a layer of copper over the seed layer using electroless plating.

2. The method of claim 1, wherein depositing a seed layer includes depositing a seed layer having a thickness of less than 15 nanometers (nm).

3. The method of claim 1, wherein depositing a seed layer includes depositing a seed layer using a physical vapor deposition process.

4. The method of claim 1, wherein using a photolithography technique in order to define a number of via holes above the seed layer includes patterning a photoresist layer to define the number of via holes above the seed layer.

5. The method of claim 4, wherein depositing a layer of copper using electroless plating includes filling the number of via holes to a top surface of the photoresist layer.

6. The method of claim 5, wherein the method further includes removing the photoresist layer using oxygen plasma ashing.

1. A method for forming vias on a substrate, comprising:

depositing a seed layer including a thin film of Palladium (Pd) or Copper (Cu) having a thickness of less than 15 nanometers (nm) on the substrate;

depositing a patterned photoresist layer over the seed layer, wherein depositing the patterned photoresist layer defines a number of via holes opening to the seed layer;

depositing a layer of copper over the seed layer using electroless plating; and

removing the photoresist layer using oxygen plasma ashing.

5. A method for forming vias on a substrate, comprising:

depositing a seed layer including a thin film of Palladium (Pd) or Copper (Cu)having a discontinuous island structure on the substrate using a sputtering deposition technique;

depositing a patterned photoresist layer over the seed layer, wherein depositing the patterned photoresist layer defines a number of via holes opening to the seed layer;

depositing a layer of copper over the seed layer using electroless plating.

6. The method of claim 5, wherein depositing a first seed layer having a discontinuous island structure includes a discontinuous island structure having a thickness of less than 15 nanometers (nm).

7. The method of claim 5, wherein depositing a layer of copper over the seed layer includes forming a number of copper vias, wherein the number of copper vias form on the seed layer but not on the patterned photoresist layer.

9. The method of claim 7, wherein forming a number of copper vias includes filling the number of via holes to a top surface of the patterned photoresist layer.

12. The method of claim 8, wherein the method further includes removing the photoresist layer using oxygen plasma ashing.

13. (Amended) A method for forming copper vias and a first metal layer, comprising:

depositing a first seed layer including a thin film of Palladium (Pd) or Copper (Cu) on a substrate;

depositing a first patterned photoresist layer, wherein depositing the first patterned photoresist layer defines a first number of via holes above the first seed layer;

forming a first layer of copper using electroless plating, wherein forming the first layer of copper vias using electroless plating includes filling the first number of via holes to a top surface of the first patterned photoresist layer;

depositing a second seed layer including a thin film of Palladium (Pd) Copper (Cu) on the first layer of copper vias and the top surface of the photoresist layer;

depositing a second patterned photoresist layer, wherein depositing the second patterned photoresist layer defines a second number of conductor line openings above the second seed layer; and

forming a second layer of copper using electroless plating, wherein depositing a second layer of copper using electroless plating includes filling the second number of conductor line openings to a top surface of the second patterned photoresist layer.

14. The method of claim 13, wherein depositing a first seed layer includes depositing a first seed layer having a discontinuous island structure.

15. The method of claim 13, wherein depositing a first seed layer includes depositing a first seed layer using an evaporation deposition technique.

13. 10
~~16.~~ The method of claim ~~13~~, wherein forming a first layer of copper using electroless plating includes forming a first number of copper vias, wherein the first number of copper vias form on the first seed layer but not on the first patterned photoresist layer.

14. 10
~~17.~~ The method of claim ~~13~~, wherein depositing the second seed layer includes depositing the second seed layer using a physical vapor deposition process.

15. 10
~~18.~~ The method of claim ~~13~~, wherein depositing a second patterned photoresist layer includes depositing a second patterned photoresist layer which has a thickness which is less that a thickness of the first patterned photoresist layer.

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16. 10
~~19.~~ (Amended) The method of claim ~~13~~, wherein depositing the second patterned photoresist layer which defines a second number of conductor line openings includes a third number of first level metal line openings.

17.
~~20.~~ (Amended) A method for forming a multilayer copper wiring structure, comprising:

depositing a first seed layer on a substrate;

patterning a first photoresist layer over the first seed layer to define a first number of via holes opening to the first seed layer;

forming a first level of copper vias in the first number of via holes using electroless plating;

depositing a second seed layer on the first level of copper vias and first photoresist layer;

patterning a second photoresist layer over the second seed layer to define a second number of conductor line openings to the second seed layer;

forming a first level of conductor lines in the second number of conductor line openings using electroless plating;

depositing a third seed layer on the first level of conductor lines and the second

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photoresist layer;

patterning a third photoresist layer over the third seed layer to define a third number of via holes opening to the third seed layer; and

forming a second level of copper vias in the third number of via holes using electroless plating.

18. 17
~~21.~~ (Amended) The method of claim ~~20~~, wherein the method further comprises:

depositing a fourth seed layer on the second level of copper vias and third photoresist layer;

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patterning a fourth photoresist layer over the fourth seed layer to define a fourth number of conductor line openings to the fourth seed layer; and

forming a second level of conductor lines in the fourth number of conductor line openings using electroless plating.

19. 18
~~22.~~ The method of claim ~~21~~, wherein depositing the first seed layer includes depositing a first seed layer having a discontinuous island structure.

20. 19
~~23.~~ The method of claim ~~22~~, wherein depositing a first seed layer having a discontinuous island structure includes depositing a discontinuous island structure of Palladium (Pd) or Copper (Cu).

21. 18
~~24.~~ (Amended) The method of claim ~~21~~, wherein forming a first level of copper vias in the third number of via holes using electroless plating includes forming the third number of copper vias on the seed layer but not on the first photoresist layer.

22. 18
~~25.~~ The method of claim ~~21~~, wherein depositing a first seed layer includes depositing a first seed layer having a thickness of less than 15 nanometers (nm).

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23. ~~26.~~ The method of claim ~~21~~ 18, wherein depositing the first seed layer includes depositing the first seed layer using a physical vapor deposition process.

24. ~~27.~~ The method of claim ~~21~~ 18, wherein patterning a second photoresist layer over the second seed layer includes patterning a second photoresist layer having a thickness which is less than a thickness of the first photoresist layer.

25. ~~28.~~ (Amended) A method for forming a multilayer copper wiring structure, comprising:

depositing a first seed layer including a thin film of Palladium (Pd) or Copper (Cu) on a substrate using a physical vapor deposition process;

B1 patterning a first photoresist layer over the first seed layer to define a first number of via holes opening to the first seed layer;

forming a first level of copper vias in the first number of via holes using electroless plating;

depositing a second seed layer on the first level of copper vias and first photoresist layer;

patterning a second photoresist layer over the second seed layer to define a second number of conductor line openings to the second seed layer;

forming a first level of copper lines in the second number of conductor line openings using electroless plating;

depositing a third seed layer on the first level of copper lines and the second photoresist layer;

patterning a third photoresist layer over the third seed layer to define a third number of via holes opening to the third seed layer;

forming a second level of copper vias in the third number of via holes using electroless plating; and

removing the first, second, and third photoresist layers using oxygen plasma etching.

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24. 25
~~29.~~ The method of claim ~~28~~, wherein depositing a first seed layer including a thin film of Palladium (Pd) or Copper (Cu) on a substrate using a physical vapor deposition process includes using an evaporation deposition technique.

27. 25
~~30.~~ The method of claim ~~28~~, wherein removing the first, second, and third photoresist layers using oxygen plasma etching includes removing the first, second, and third seed layers.

28. 25
~~31.~~ The method of claim ~~28~~, wherein depositing a second and a third seed layer includes depositing a second and third seed layer having a discontinuous island structure.

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29. 31
~~32.~~ The method of claim ~~31~~, wherein depositing a second and a third seed layer having a discontinuous island structure includes depositing a second and a third seed layer using a sputtering deposition technique.

30. 29
~~33.~~ The method of claim ~~32~~, wherein depositing a second and a third seed layer includes depositing a second and a third seed layer having a thickness of less than 15 nanometers (nm).

31.
~~34.~~ (Amended) A method for forming a multilayer copper wiring structure, comprising:

depositing a first seed layer including a thin film of Palladium (Pd) or Copper (Cu) on a substrate;

patterning a first photoresist layer over the first seed layer to define a first number of via holes opening to the first seed layer;

forming a first level of copper vias in the first number of via holes using electroless plating;

depositing a second seed layer including a thin film of Palladium (Pd) or Copper (Cu) on the first level of copper vias and first photoresist layer;

patterning a second photoresist layer over the second seed layer to define a second

number of conductor line openings to the second seed layer;

forming a first level of copper lines in the second number of conductor line openings using electroless plating;

depositing a third seed layer including a thin film of Palladium (Pd) or Copper (Cu) on the first level of copper lines and the second photoresist layer;

patterning a third photoresist layer over the third seed layer to define a third number of via holes opening to the third seed layer; and

forming a second level of copper vias in the third number of via holes using electroless plating;

depositing a fourth seed layer including a thin film of Palladium (Pd) or Copper (Cu) on the second level of copper vias and third photoresist layer;

patterning a fourth photoresist layer over the fourth seed layer to define a fourth number of conductor line openings to the fourth seed layer; and

forming a second level of copper lines in the fourth number of conductor line openings using electroless plating.

32. ~~35.~~ The method of claim ~~34~~ 31, wherein the depositing the first, second, third, and fourth seed layers includes depositing a first, second, third, and fourth seed layer having a discontinuous island structure.

33. ~~36.~~ The method of claim ~~35~~ 32, wherein depositing a first, second, third, and fourth seed layer having a discontinuous island structure includes depositing a first, second, third, and fourth seed layer using a sputtering deposition technique.

34. ~~37.~~ The method of claim ~~36~~ 33, wherein depositing a first, second, third, and fourth seed layer having a discontinuous island structure includes depositing a first, second, third, and fourth seed layer having thickness of less than 10 nanometers (nm).

~~38~~ 36. The method of claim ~~34~~ 31, wherein the method further includes removing the first, second, third, and fourth photoresist layers using an oxygen plasma etching.

~~39~~ 36. The method of claim ~~38~~ 35, wherein removing the first, second, third, and fourth photoresist layers using an oxygen plasma etching includes removing the first, second, third, and fourth seed layers.

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~~40~~ 37. (Amended) The method of claim ~~39~~ 34, wherein the further includes forming a thin diffusion barrier on the first number of via holes and on the third number of via holes and on the first level and the second level of copper lines.

~~41~~ 38. The method of claim ~~40~~ 37, wherein forming a thin diffusion barrier includes forming a thin diffusion barrier of Tungsten Silicon Nitride (WSi_xN_y) having a thickness of less than 8 nanometers (nm).

~~42~~ 39. The method of claim ~~41~~ 38, wherein forming a thin diffusion barrier of Tungsten Silicon Nitride (WSi_xN_y) having a thickness of less than 8 nanometers (nm) includes forming a graded composition of WSi_x, where x varies from 2.0 to 2.5, and nitriding the graded composition of WSi_x.

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~~65~~ 4. (New) The method of claim 1, wherein depositing a seed layer includes forming a discontinuous seed layer having island structures with the island structures having a thickness in a range of 3 to 10 nanometers.